Reg.No.:								

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
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Question Paper Code: 7012

B.E. / B.Tech. DEGREE SUPPLEMENTARY EXAMINATIONS – FEB. / MAR. 2020
Third Semester
Computer Science and Engineering
U15EC305 – DIGITAL LOGIC DESIGN
(Common to Information Technology)
(Regulation 2015)

Time : Three Hours Maximum : 100 Marks

Answer ALL the questions

PART – A

(10 x 2 = 20 Marks)

1. State De Morgan's theorem.
2. Convert the hexadecimal number ABCD to binary.
3. State the limitations of karnaugh map.
4. Convert the given expression in canonical SOP form Y = AC + AB + BC.
5. Write the function of magnitude comparator.
6. Compare the function of Encoder and Decoder.
7. Write the differences between synchronous and asynchronous counters.
8. Derive the flip-flop excitation table for D flip-flop.
9. Differentiate between Moore's and mealy's model.
10. When does race condition occur?

PART – B

(5 x 13 = 65 Marks)

11. a) i. State and prove any 3 laws of Boolean Algebra. (6)
ii. Apply Boolean algebra to simplify the expression and realize using only NAND gates. Y = (AB + C') D + EF. (7)

(OR)

b) i. Convert the hexadecimal number $B5_{(16)}$ to decimal and octal.(4)

ii. Reduce the following Boolean expressions to the indicated number of literals:

a. A'C' + ABC + AC' to three literals (2)

b. (x'y'+z)' + z + xy + wz to three literals (2)

c. A'B(D'+C'D) + B(A+A'CD) to one literal (3)

d. (A'+C)(A'+C')(A+B+C'D) to four literals (2)

12. a) Find all the prime implicants for the following Boolean function (using K-Map) and determine which are essential and implement with NAND gates.

$$F(w, x, y, z) = \sum(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14).$$

(OR)

b) Minimize f(A, B, C, D) = (0, 1, 2, 3, 5, 7, 8, 10, 12, 13, 15) using Quine-McCluskey method.

13. a) i. Design a full subtractor using 1-to-8 Demultiplexer. (6)

ii. Design a 4-bit Magnitude Comparator with logic diagram. (7)

(OR)

b) Implement the following function using PAL.

i. W (A, B, C, D) = $\sum$m (2, 12, 13) (4)

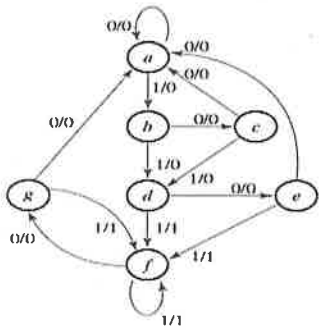
ii. X (A, B, C, D) = $\sum$m (7, 8, 9, 10, 11, 12, 13, 14, 15) (3)

iii. Y (A, B, C, D) = $\sum$m (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15) (3)

iv. Z (A, B, C, D) = $\sum$m (1, 2, 8, 12, 13) (3)

14. a) i. With relevant diagram explain the working of master-slave JK flip flop. (5)

ii. Evaluate the following state diagram and tabulate the reduced state table. Consider the input sequence 01010110100 starting from the initial state a. (8)



(OR)

b) Design a mod-5 up/down counter using JK-FF. Draw the realization diagram.

15. a) Illustrate how to avoid races, cycles in asynchronous sequential circuits with suitable examples.

(OR)

b) i. Explain the types of hazards in sequential circuits with examples. (7)

ii. Write a technical note on "Design of asynchronous sequential circuits". (6)

PART – C

(1 x 15 = 15Marks)

16. a) Draw state transition diagram of sequence detector circuit that detects 1101 from input data stream using both Mealy and Moore model.

(OR)

b) i. Design a gated latch circuit which have two inputs G and D and one output Q. The output Q retains its previous state value if the input G = 0 regardless of the input D. The output Q will follow the input D if the gated Latch input G = 1. (7)

ii. Simplify the function F using K-map where $F = \pi (0, 1, 4, 5, 13)$ (8)